memory, said signal paths capable of moving sets of said system operation signals at system operation clock rates, said sets of system operation signals stored in said memory so that said sets of system operation signals are retrievable.

10. (Amended twice) An integrated circuit comprising

an interface for coupling to an external diagnostic processor;

a unit responsive to instructions from said external diagnostic processor for capturing sets of sequential system operation signals of said integrated circuit;

a plurality of probe lines coupled to said unit for carrying said system operation signals at predetermined probe points of said integrated circuit, wherein said probe lines comprise strings of storage elements providing signal paths between said probe points and said unit, said signal paths capable of moving said sets of sequential system operation signals at system operation clock rates;

a memory coupled to said unit and to said interface, said sets of sequential system operation signals stored in said memory at one or more clock signal rates internal to said integrated circuit and retrieved from said memory through said interface to said external process at one or more clock signal rates external to said integrated circuit so that said external diagnostics processor can process said captured system operation signals.

15. (Amended twice) A method of operating an integrated circuit having logic blocks, a control unit, a memory and a plurality of probe lines of said logic blocks, said method comprising

operating said logic blocks to perform normal system operations at one or more system clock signal rates internal to said integrated circuit;

enabling said probe lines responsive to said control unit to capture and carry sets of system operation signals of said logic blocks at said system clock signal rates internal to said integrated circuit;

retrieving said sets of system operation signals from said logic blocks along said probe lines at said system clock signal rates internal to said integrated circuit,

storing said sets of system operation signals in said memory at said system clock signal rates internal to said integrated circuit; and

processing said sets of stored system operation signals to perform test and debug operations of said logic blocks of said integrated circuit.

REMARKS

Reconsideration of the present patent application, as amended, is respectfully requested.

Of previously pending claims 1-15, all were rejected. The applicants believe that claims 16-22 are also pending since the present Office Action refers to applicants' Amendment, filed January 2, 2001, in which new claims 16-22 were added. The applicants assume that reference to claims 16-22 were inadvertently omitted in the Office Action.

Substantively, claims 1, 3-4, and 10 were rejected under 35 USC §103(a) as being obvious over U.S. Patent No. 5,991,898, which issued November 23, 1999 to J. Rajski *et al.* in view of U.S. Patent No. 5,206,862, which issued April 27, 1993 to S. Chandra *et al.* Claims 2, 5-9 and 15 were rejected under 35 USC §103(a) as being unpatentable over the cited Rajski patent in view of the cited Chandra patent and further in view of U.S. Patent No. 6,003,142, which issued December 14, 1999 to J. Mori.

For the purposes of brevity, the applicants argue the patentability of independent claims 1, 10 and 15. It is understood that dependent claims 2-9, 11-14, and 16-22 should be considered patentable for at least being dependent upon allowable base claims.

With respect to claims 1 and 10, the Examiner has stated that Rajski *et al.* teaches "a plurality of scan lines" and further that Chandra *et al.* teaches "a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points of said logic blocks." The Examiner then concluded, "It would be obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Rajski to provide a built-in self test of multiple scan based integrated [circuit (sic)] having plurality of probe lines for carrying system operation signals at predetermined probe points as taught by Chandra. This modification would be obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide test signals to select test points while response are sensed...."